REMARKS

This paper responds to the Advisory Action mailed on March 28, 2006 and the Final Office Action mailed December 28, 2005.

Claims 11, 15, 18, 22, 25, 35 and 41 are amended, no claims are canceled, and no claims are added; as a result, claims 11-25, 35-39 and 41-43 are now pending in this application.

§103 Rejection of the Claims

Claims 11-16, 18-25, 35-38 and 41-43 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Boruta (EP 0 678 901) in view of Altavela et al. (U.S. 5,408,739) with Arlt et al. (U.S. 4,804,641).

As discussed in the previous response, Boruta discloses a method of sawing or cutting a wafer that has deposited material 32 in the scribe lines wider than the saw blade (see col. 1, lines 26-30). There are three saw cuts, first groove 36, spaced apart parallel second groove 38, and third groove 39 overlapping the first two cuts (see figure 2A-D and figure 3A-D; and col. 3, lines 34-50). Thus the scribe lane is not a "blank" region, as recited in the present claims. Applicant respectfully submits that there is no suggestion in Boruta of having the scribe cuts near the edge of the device circuit regions and one of ordinary skill would know that the disclosed saw blade would be placed in the approximate middle of the scribe lane, since otherwise the size of the adjacent die would be increased. Thus, it is respectfully submitted that one of ordinary skill would know that a saw thickness of 1.2 to 1.6 mil (col. 2, line 58) would result in a distance to the circuit edge of about 15 to 25 microns, on the average.

Altavela is used in the outstanding Office Action to show that further polishing may not be required. Altavela discloses sawing the front surface of a thermal ink jet printer head so that the sawing leaves a front surface that does not require a polishing step (see Fig. 8 and col. 1, lines 7-14). However, Applicant respectfully submits that there is not proper motivation given to combine an ink jet reference with a saw reference to obtain a ground or polished surface with a specific location relative to the active circuitry area.

Arit discloses al ring of specially grown thermal oxide surrounding the active area of a chip to act as a crack stopper and prevent the wafer sawing from producing edge chips penetrating the active area. Arit is used in the outstanding Office Action to show that it is known in the art that wafer sawing creates cracks. Applicant agrees that it is known that sawing creates edge cracks, but notes that there is no suggestion in any of the cited references to suggest a solution to the problem, other than growing a crack stopper region, which as noted in the previous response, increases the size of the die, which would seem to teach against the present embodiments. The Arit separately grown oxide ring is greater than 5 microns and has a safety region that is also greater than 5 microns (see figure 2 and col.3, lines 13-29).

Applicant respectfully submits that the suggested combination of references does not provide proper motivation for one of ordinary skill in the art to combine their teachings to reduce the size of the die, at least because there is no suggestion in any of the cited references to reduce the size of the die. Thus the suggested combination is improper as lacking motivation to combine, since none of the references are addressed to, or suggest reducing the scribe line to circuitry distance.

Even if there were proper motivation to make the suggested combination, the result would still not obtain the claimed features. Specifically, the suggested combination neither describes nor suggests at least the feature of "*...a top portion of each individual planar perimeter side surface disposed in the second region and within approximately 5 microns of an edge of a metal feature of the first region ...*", as recited in independent claim 11, as amended herein, with similar language in the other independent claims. The cited references do not provide any disclosure of an edge that is within 5 microns of active device regions, nor within 5 microns of a metal feature edge, nor that "*... each planar perimeter side surface of the semiconductor die being a flat surface substantially perpendicular to the first planar surface...*", as recited in claim 11. This feature is found in the original claims and the specification at least at Figures 2 and 3, and at page 5, line 27.

The dependent claims are felt to be in patentable condition at least as depending from base claims shown above to be patentable over the references. In light of the above noted claims amendments, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney David Suhl at (508) 865-8211, or the undersigned attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

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Date 27 April '06

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 27 day of April, 2006.

Name

Signature